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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,920	03/22/2004	Steven A. Wright	0516-02	9685

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EXAMINER	
BENNETT, ZAHRA I	

ART UNIT	PAPER NUMBER
2875	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/805,920	WRIGHT ET AL.	
	Examiner	Art Unit	
	Zahra Bennett	2875	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-13,and 15* is/are rejected.

7)☒ Claim(s) *6 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *22 March 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hochstein (US Patent 5,782,555).

With respect to claim 1, Hochstein discloses a substrate adapted for mounting a light-emitting diode (LED), the substrate comprising: a circuit board (26) having opposed first and second surfaces, the circuit board being constructed of an electrically insulating material (Column 4, lines 1-2); a pair of electrical lead pads adapted for mounting the LED on the first surface of the circuit board (Figure 4: 30,32); a heat dissipating structure having: an LED thermal pad adapted to abut the LED when the LED is mounted on the pair of electrical lead pads (Figure 6: 34, see Column 4, lines 4-8); and a heat dissipation region extending from and thermally coupled to the LED thermal pad (Figures 3 and 4: 36a); and a thermally conductive plating (Figure 4: 50) disposed directly on the second surface of the circuit board opposite the heat dissipation region (see Column 4, lines 28-34).

Hochstein does not teach that the heat dissipation structure, which has an LED thermal pad and a heat dissipation region, is disposed on the first surface of the board.

It would have been obvious to one of ordinary skill at the time of the invention to have a heat dissipation structure disposed on the first surface of the circuit board. One would have been motivated to modify the device of Hochstein for the benefit of conducting heat directly to the light emitting side of the assembly.

Hochstein discloses that the heat dissipation region (Figure 3: 36a) having at least twice the area of the LED thermal pad (Figure 6: 34). Hochstein discloses the heat dissipating structure includes an isolated region that is electrically isolated from the heat dissipation region, the isolated region having a plurality of heat conducting vias that extend through the circuit board and are thermally coupled with the thermally conductive region (Column 4: 28-32, also Column 7, lines 7-11). Hochstein further discloses vias that are electrically isolated from the heat dissipating structure by a non-electrically-conductive region (Figure 2: 56). Hochstein also teaches that the vias are copper plated through-holes (Column 7, lines 3-7).

Claims 3, 5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hochstein as applied to claims 1 and 4 above, in further view of Gasquet et al. (US Patent 6,821,143).

With respect to claim 3, Hochstein does not teach the heat dissipation region including first and second sides. Gasquet teaches that the heat dissipation region includes first and second regions (Figure 5: 8a and 8b) extending from opposite sides of the LED thermal pad. It would have been obvious to one of ordinary skill at the time of

the invention to include first and second regions of the thermal pad for the benefit of having two separate regions that are able to conduct heat across the LED.

With respect to claim 5, Hochstein does not teach vias arranged in spokes that extend outwardly. Gasquet teaches holes (Figure 4: 14) arranged in spokes (12b) that extend outwardly from the LED thermal pad. It would have been obvious to one of ordinary skill at the time of the invention to arrange the vias in the device of Hochstein within the spokes in the device of Gasquet. One would be motivated to modify the device for the benefit of transferring heat adequately from the lead to the thermal conductive plating.

With respect to claim 7, Hochstein does not teach the vias and the heat dissipation region are thermally connected with a conductive bridge layer opposite the circuit board. Gasquet teaches that the vias and the heat dissipation region are thermally connected with a conductive bridge layer opposite the circuit board (Figure 5, see Column 3, lines 13-14), the conductive bridge layer being electrically isolated from the vias and/or the heat dissipation region by a dielectric layer (10b). It would have been obvious to one of ordinary skill at the time of the invention to have the vias and the heat dissipation region are thermally connected with a conductive bridge layer opposite the circuit board, the conductive bridge layer being electrically isolated from the vias and/or the heat dissipation region by a dielectric layer for the benefit of connecting the two legs of the heat dissipating region so the heat can be dissipated effectively.

Claims 9, 10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hochstein '555 as applied to claim 1 above, and further in view of Hochstein (US Patent 6,428,189). Hochstein '555 discloses that the heat dissipation region (Figure 3: 36a) having at least twice the area of the LED thermal pad (Figure 6: 34). Hochstein '555 discloses the heat dissipating structure includes an isolated region that is electrically isolated from the heat dissipation region, the isolated region having a plurality of heat conducting vias that extend through the circuit board and are thermally coupled with the thermally conductive region (Column 4: 28-32, also Column 7, lines 7-11). Hochstein '555 further discloses vias that are electrically isolated from the heat dissipating structure by a non-electrically-conductive region (Figure 2: 56). Hochstein '555 also teaches that the vias are copper plated through-holes (Column 7, lines 3-7).

With respect to claim 9, Hochstein '555 discloses a substrate adapted for mounting a light-emitting diode (LED), the substrate comprising: a circuit board (26) having opposed first and second surfaces, the circuit board being constructed of an electrically insulating material (Column 4, lines 1-2); a pair of electrical lead pads adapted for mounting the LED on the first surface of the circuit board (Figure 4: 30,32); a heat dissipating structure having: an LED thermal pad adapted to abut the LED when the LED is mounted on the pair of electrical lead pads (Figure 6: 34, see Column 4, lines 4-8); and a heat dissipation region extending from and thermally coupled to the LED thermal pad (Figures 3 and 4: 36a); and a thermally conductive plating (Figure 4:

50) disposed directly on the second surface of the circuit board opposite the heat dissipation region (see Column 4, lines 28-34).

Hochstein does not teach that the heat dissipation structure, which has an LED thermal pad and a heat dissipation region, is disposed on the first surface of the board. It would have been obvious to one of ordinary skill at the time of the invention to have a heat dissipation structure disposed on the first surface of the circuit board. One would have been motivated to modify the device of Hochstein for the benefit of conducting heat directly from the light emitting side of the assembly.

In addition, Hochstein '555 does not teach the substrate further comprising LEDs that are electrically connected in series via a circuit electrically isolated from the heat dissipating structures. Hochstein '189 teaches the substrate further comprising LEDs that are electrically connected in series via a circuit electrically isolated from the heat dissipating structures (Column 5, lines 36-40). It would have been obvious to one of ordinary skill at the time of the invention to electrically connect the LEDs of Hochstein '555 in series for the benefit of isolating the heat sink element of each LED so the circuit does not experience a shortage, as taught by Hochstein '189.

Claims 11, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hochstein '555 and Hochstein '189 as applied to claims 9 and 12 above, in further view of Gasquet et al. (US Patent 6,821,143).

With respect to claim 11, Hochstein '555 and Hochstein '189 do not teach the heat dissipation region including first and second sides. Gasquet teaches that the heat dissipation region includes first and second regions (Figure 5: 8a and 8b) extending from opposite sides of the LED thermal pad. It would have been obvious to one of ordinary skill at the time of the invention to include first and second regions of the thermal pad for the benefit of having two separate regions that are able to conduct heat across the LED.

With respect to claim 13, Hochstein '555 and Hochstein '189 do not teach vias arranged in spokes that extend outwardly. Gasquet teaches holes (Figure 4: 14) arranged in spokes (12b) that extend outwardly from the LED thermal pad. It would have been obvious to one of ordinary skill at the time of the invention to arrange the vias in the device of Hochstein within the spokes in the device of Gasquet. One would be motivated to modify the device for the benefit of transferring heat adequately from the lead to the thermal conductive plating.

With respect to claim 15, Hochstein '555 and Hochstein '189 do not teach the vias and the heat dissipation region are thermally connected with a conductive bridge layer opposite the circuit board. Gasquet teaches that the vias and the heat dissipation region are thermally connected with a conductive bridge layer opposite the circuit board (Figure 5, see Column 3, lines 13-14), the conductive bridge layer being electrically isolated from the vias and/or the heat dissipation region by a dielectric layer (10b). It

would have been obvious to one of ordinary skill at the time of the invention to have the vias and the heat dissipation region are thermally connected with a conductive bridge layer opposite the circuit board, the conductive bridge layer being electrically isolated from the vias and/or the heat dissipation region by a dielectric layer for the benefit of connecting the two legs of the heat dissipating region so the heat can be dissipated effectively.

Allowable Subject Matter

Claims 6 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zahra Bennett whose telephone number is 571-272-2267. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Renee Luebke can be reached on 571-272-2009. The fax phone number for the organization where this application or proceeding is assigned is 571-273-2267.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RENEE LUEBKE
PRIMARY EXAMINER